LISTING OF CLAIMS:

The present listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a trench having an inner wall in a substrate;

forming an insulation film on the inner wall of the trench;

forming a conductive film in the trench on the insulation film; ~~and~~

forming an interlayer over the conductive film; and

annealing the substrate for improvement of reliability of the insulation film at an annealing temperature after the step of forming the conductive film so that a damage in the insulation film is removed at the annealing temperature,

wherein the substrate is made of silicon, ~~and~~

wherein the annealing temperature is higher than 1150 degrees Celsius and is equal to or less than 1200 degrees Celsius, and

wherein the annealing of the substrate is performed prior to forming the interlayer.

2. (Original) The method according to claim 1, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

3. (Cancelled)

4. (Previously Presented) The method according to claim 1, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

5. (Original) The method according to claim 1,

wherein the conductive film is made of doped poly crystalline silicon, and

wherein the insulation film is made of silicon oxide and silicon nitride.

6. (Original) The method according to claim 5, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

7. (Original) The method according to claim 1,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the trench includes a sidewall and upper and lower portions,

wherein the oxide-nitride-oxide film is disposed on the sidewall of the trench, the upper oxide film is disposed on the upper portion of the trench, and the lower oxide film is disposed on the lower portion of the trench,

wherein the oxide-nitride-oxide film includes a silicon oxide film, a silicon nitride film and another silicon oxide film, and

wherein the upper and lower oxide films are made of silicon oxide.

8. (Original) The method according to claim 7, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

9. (Original) The method according to claim 1,

wherein the device includes a cell region and a gate lead wire region,

wherein the cell region includes a plurality of cells, each of which works as a transistor, and

wherein the gate lead wire region includes a gate lead wire.

10. (Original) The method according to claim 9,

wherein the transistor is an N channel type MOSFET, a P channel type MOSFET or an IGBT.

11. (Currently Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a trench having an inner wall in a substrate;

forming an insulation film on the inner wall of the trench;

forming a gate electrode in the trench on the insulation film;

implanting an impurity into the substrate with using the gate electrode as a mask after the step of forming the gate electrode;

performing a thermal diffusion process for diffusing the impurity so that a source region adjacent to the trench and disposed on a surface of the substrate is formed; and

annealing the substrate for improvement of reliability of the insulation film at an annealing temperature after the step of forming the conductive film so that a damage in the insulation film is removed at the annealing temperature,

wherein the substrate is made of silicon, ~~and~~

wherein the annealing temperature is higher than 1150 degrees Celsius and is equal to or less than 1200 degrees Celsius, and

wherein the annealing is performed prior to performing the thermal diffusion process.

12. (Original) The method according to claim 11,

wherein the thermal diffusion process is performed at a process temperature, and

wherein the annealing temperature in the step of annealing is higher than the process temperature in the step of performing the thermal diffusion process.

13. (Original) The method according to claim 11,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the trench includes a sidewall and upper and lower portions,

wherein the oxide-nitride-oxide film is disposed on the sidewall of the trench, the upper oxide film is disposed on the upper portion of the trench, and the lower oxide film is disposed on the lower portion of the trench,

wherein the oxide-nitride-oxide film includes a silicon oxide film, a silicon nitride film and another silicon oxide film, and

wherein the upper and lower oxide films are made of silicon oxide.

14. (Original) The method according to claim 13, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

15. (Previously Presented) The method according to claim 14,

wherein the distance between the edge of the canopy and the edge of the opening of the trench is in a range between 0.05 micrometers and 0.1 micrometers.

16. (Previously Presented) The method according to claim 11,

wherein the substrate is annealed in an inert gas atmosphere in the step of annealing.

17-25. (Canceled)

26. (Previously Presented) The method according to claim 1, further comprising forming an oxide film on the conductive film before the annealing of the substrate.

27. (Previously Presented) The method according to claim 26, wherein the oxide film covers the conductive film and the substrate.

28. (Previously Presented) The method according to claim 27, wherein the annealing of the substrate is performed for a predetermined time in a range between 10 minutes and 30 minutes.

29. (Previously Presented) The method according to claim 11, further comprising forming an oxide film on the conductive film before the annealing of the substrate.

30. (Previously Presented) The method according to claim 29, wherein the oxide film covers the conductive film and the substrate.

31. (Previously Presented) The method according to claim 30, wherein the annealing of the substrate is performed for a predetermined time in a range between 10 minutes and 30 minutes.

32. (New) The method according to claim 1, wherein the interlayer comprises borophosphosilicate glass

34. (New) The method according to claim 2, wherein the annealing is performed prior to forming the source region.

35. (New) The method according to claim 2, wherein the source region is an N^+ source region.

36. (New) The method according to claim 2, further comprising forming a body region in the substrate and adjacent to the source region.

37. (New) The method according to claim 36,

wherein the source region is an N^+ type source region, and

wherein the body region is a P type body region.

38. (New) The method according to claim 11, wherein the source region is an N^+ source region.

39. (New) The method according to claim 11, wherein the performing of the thermal diffusion process for diffusing the impurity also operates so that a body region is formed adjacent to the source region in the substrate.

40. (New) The method according to claim 39, wherein the annealing is performed prior to performing the thermal diffusion process.

41. (New) The method according to claim 40,

wherein the source region is an N^+ type source region, and

wherein the body region is a P type body region.

42. (New) The method according to claim 11, further comprising

forming an interlayer over the gate electrode,

wherein the annealing of the substrate is performed prior to forming the interlayer

43. (New) The method according to claim 42, wherein the interlayer comprises borophosphosilicate glass.